

FIG. 2

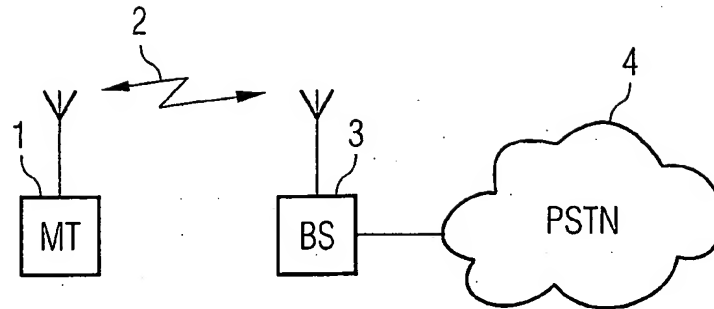


FIG. 3

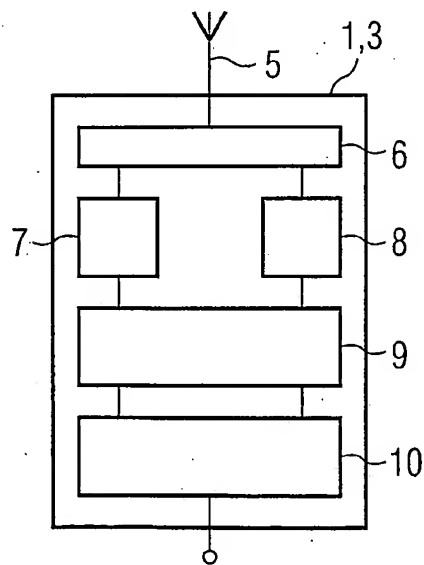
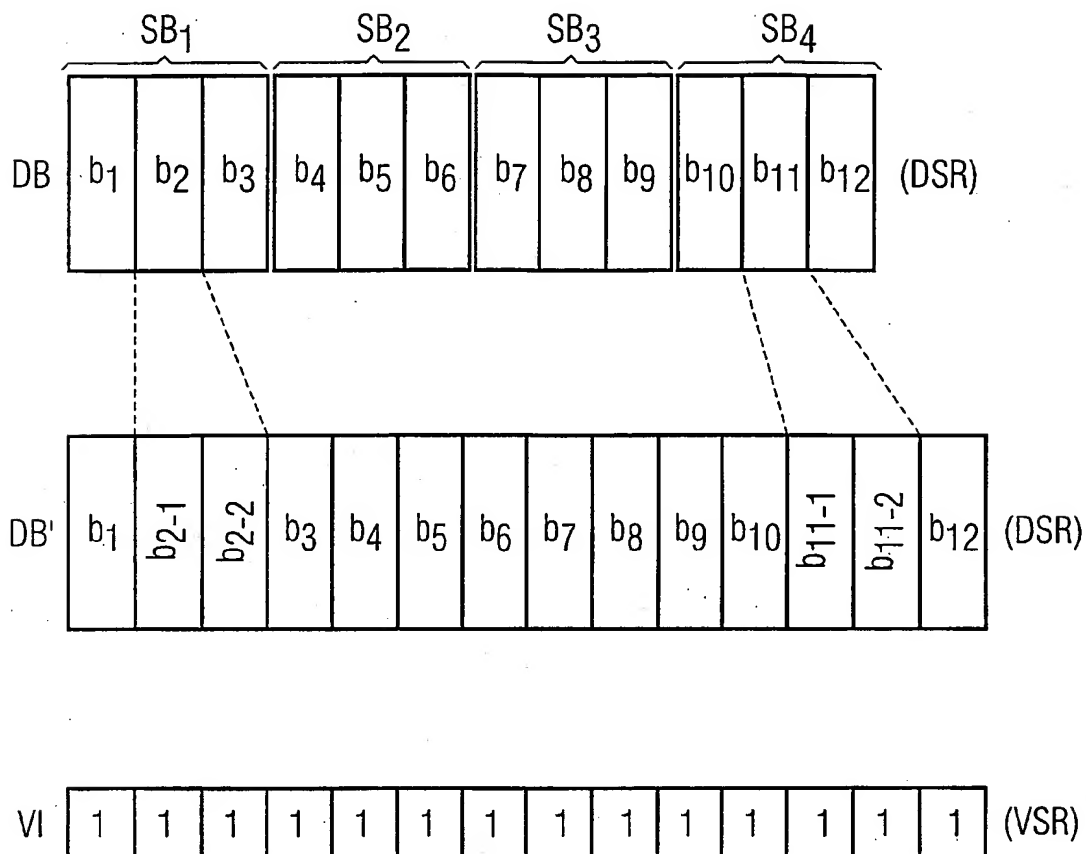
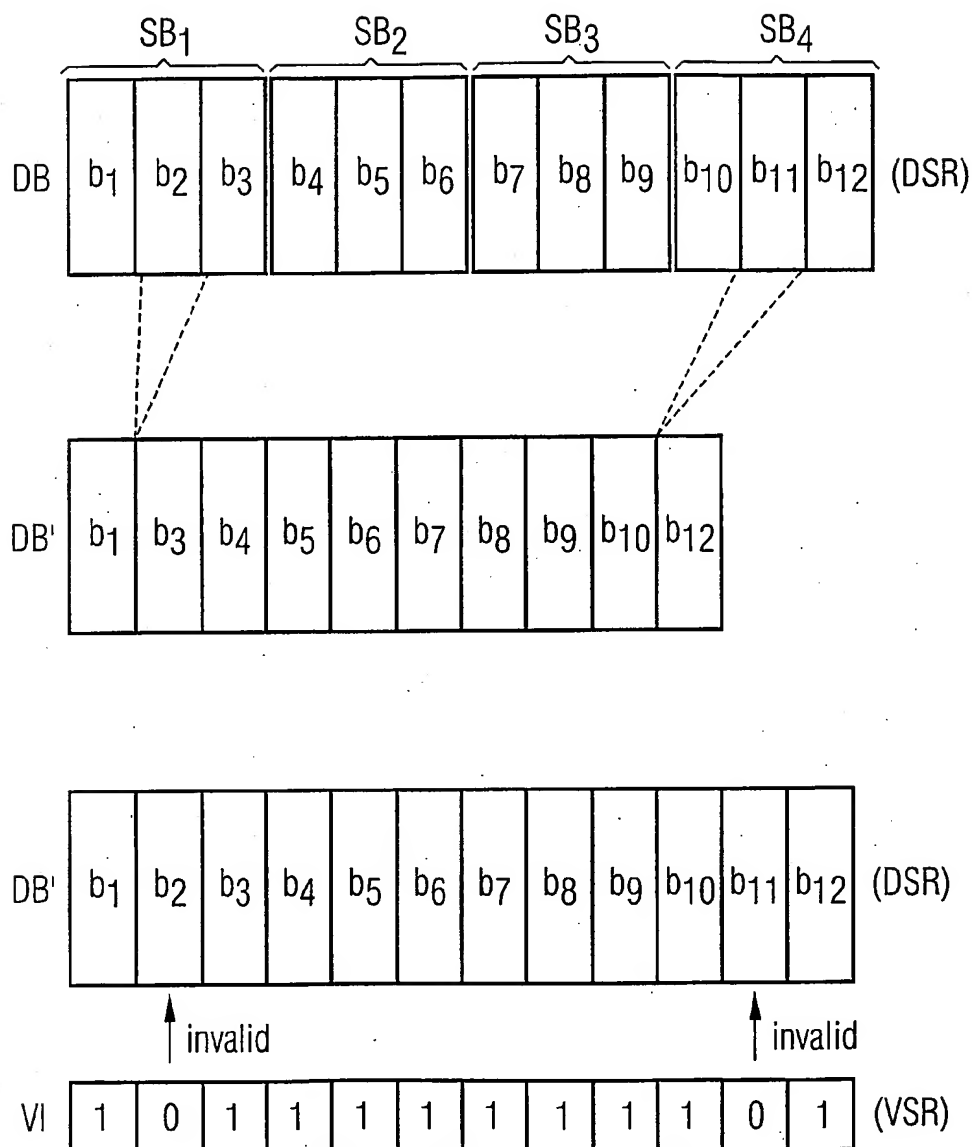


FIG. 4



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FIG. 5



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FIG. 6

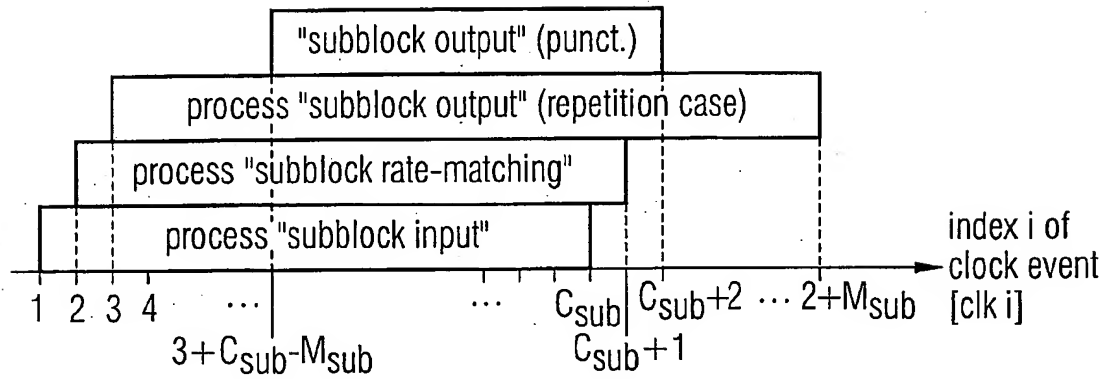
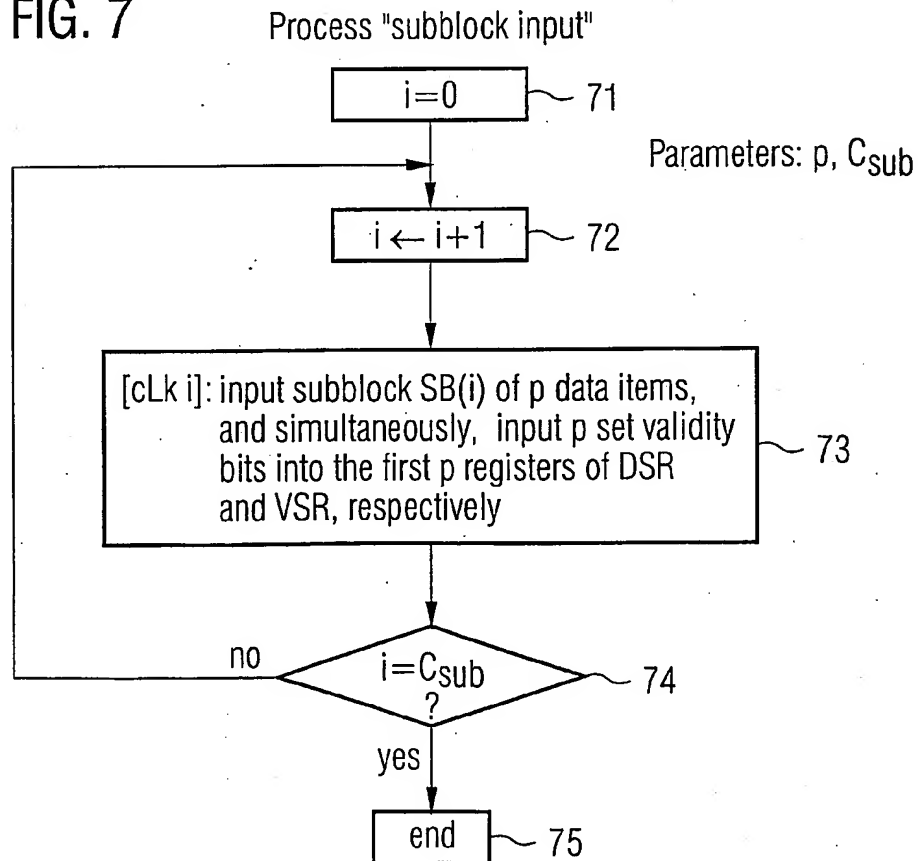


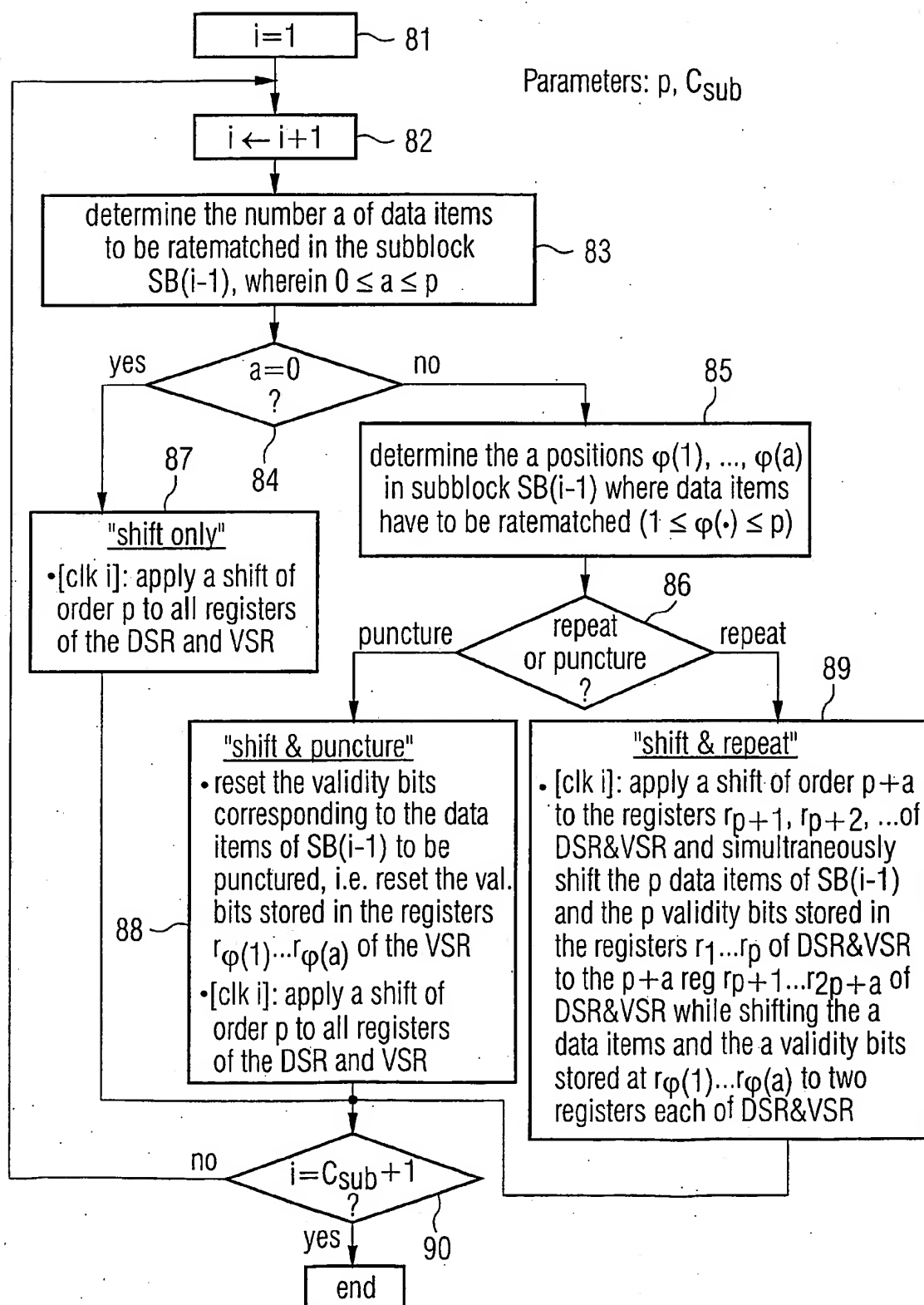
FIG. 7



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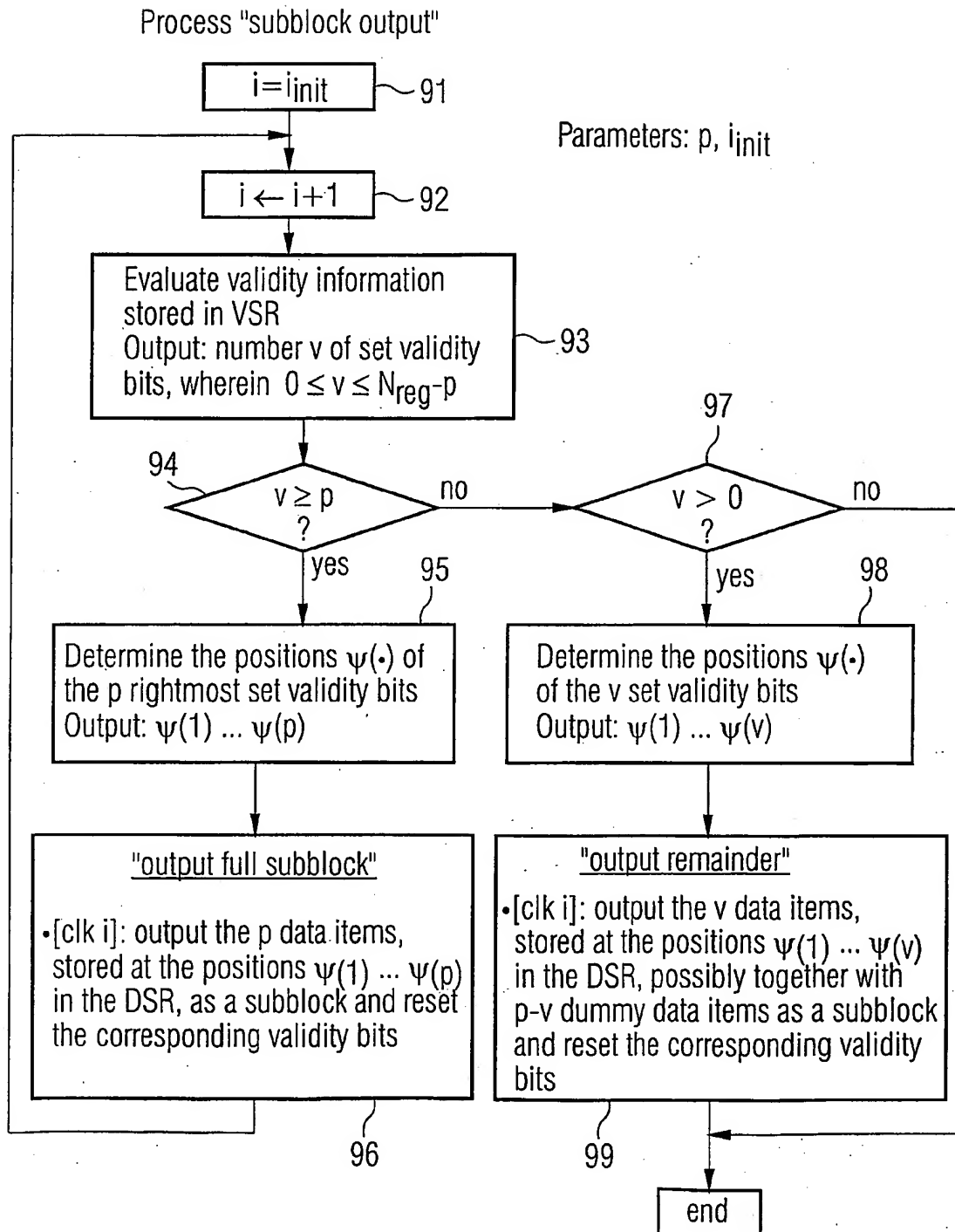
FIG. 8

Process "subblock rate matching"



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FIG. 9



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FIG.10

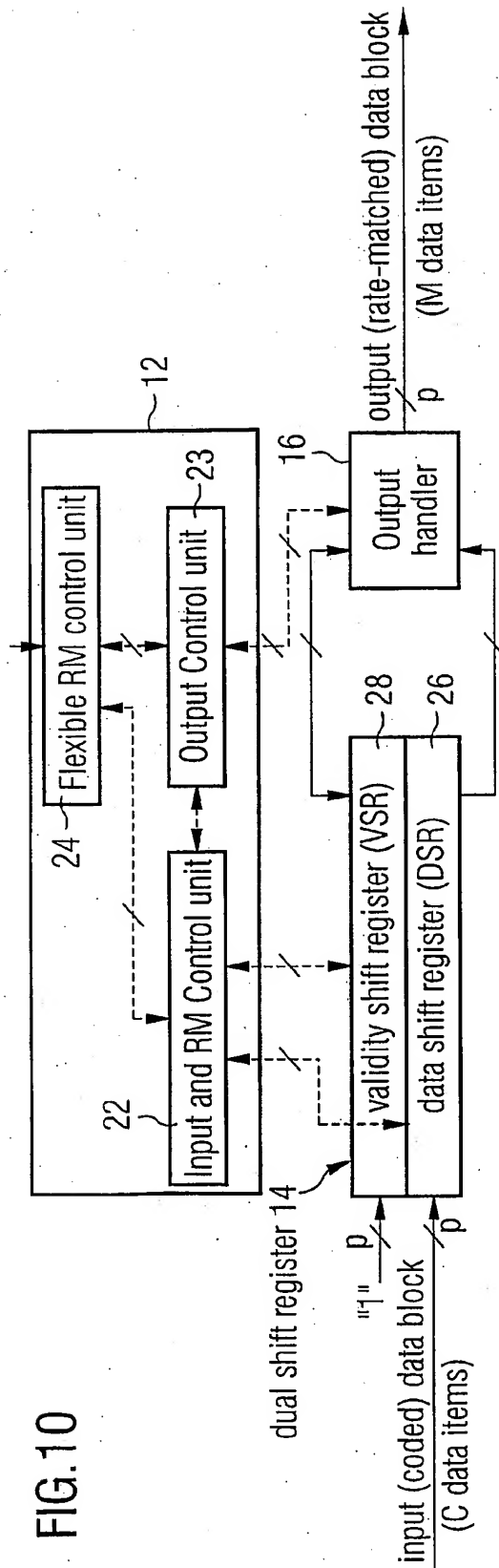
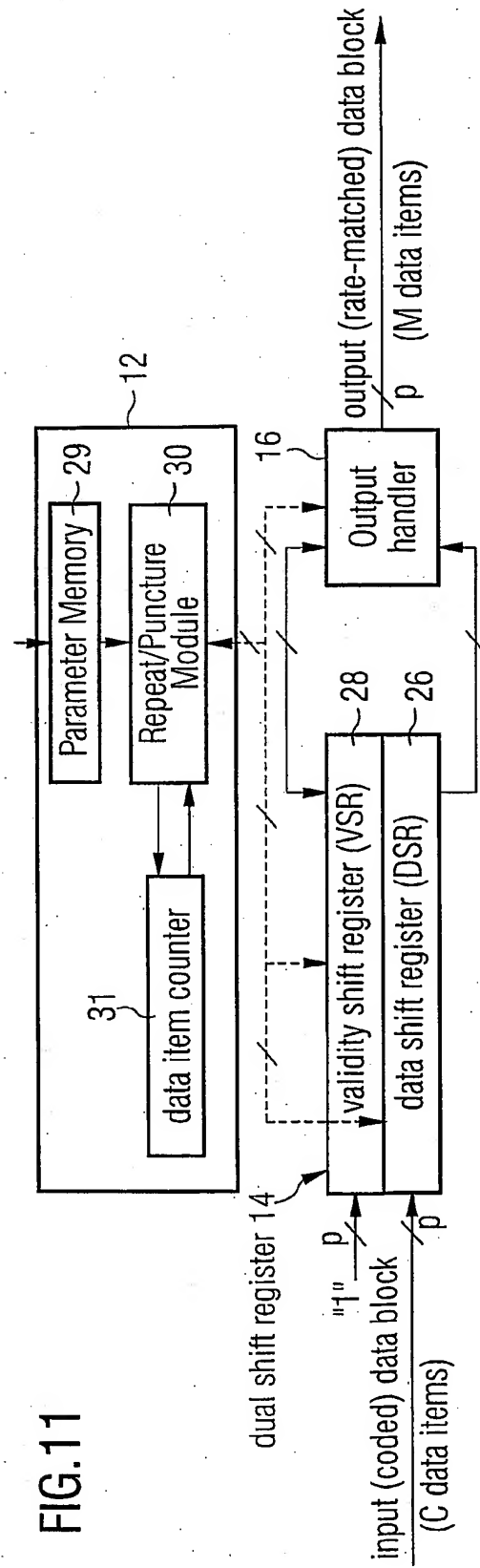


FIG.11



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FIG.12a

Shift operations only (no rate-matching required in SB(i))

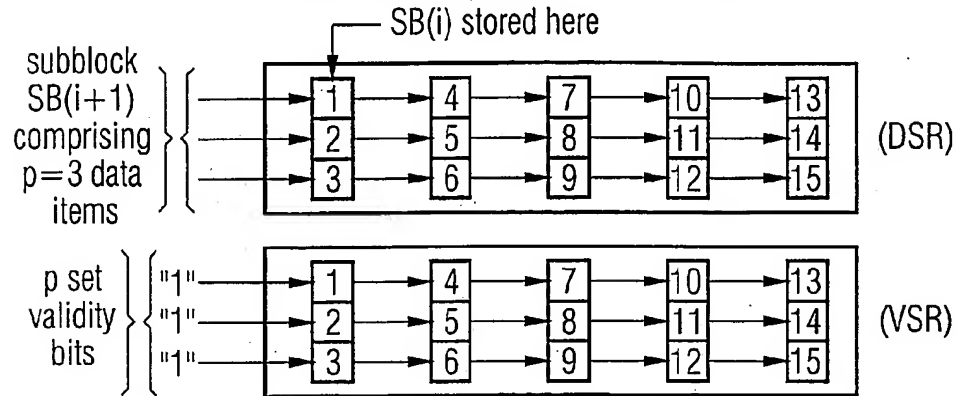


FIG.12b

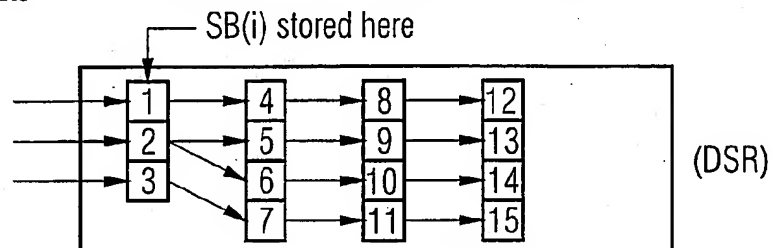
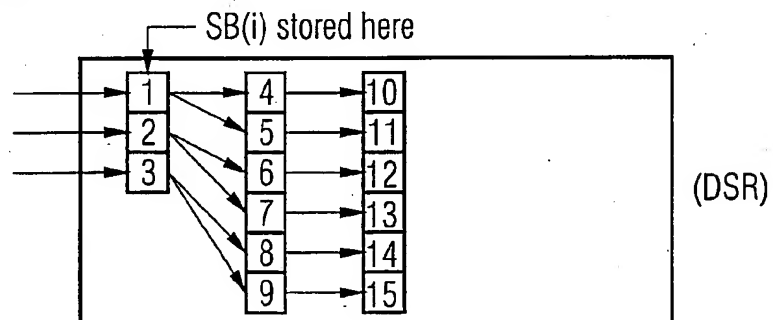
Repetition of $a=1$ data item of SB(i)

FIG.12c

Repetition of $a=3$ data items of SB(i)

- Legend:**
- : register (memory location) of DSR and VSR, respectively
 - : j-th register of DSR/VSR (r_j)
 - : shift from register j to register k at $[\text{clk } i+1]$
 - : shift from register j to register k and l (repetition) at $[\text{clk } i+1]$

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FIG.13

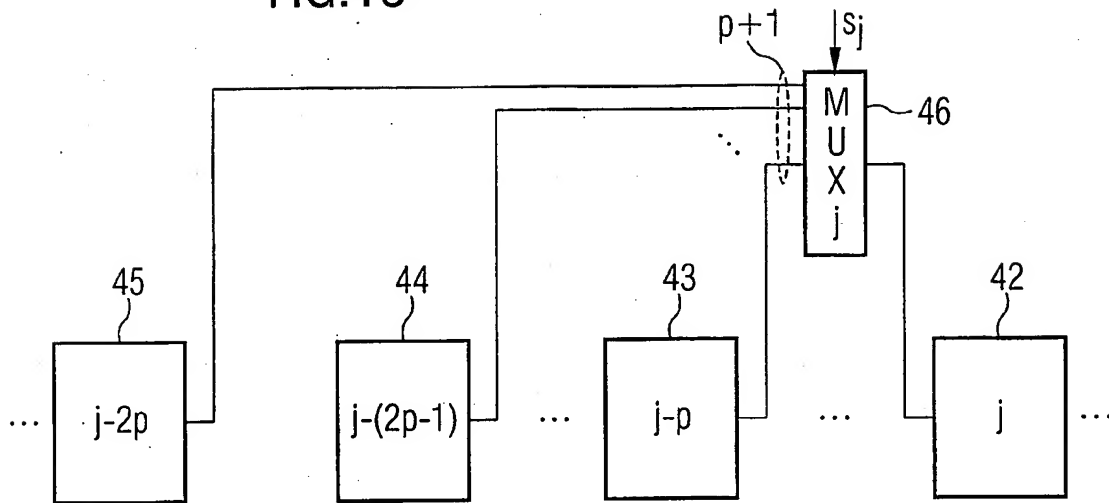


FIG.15

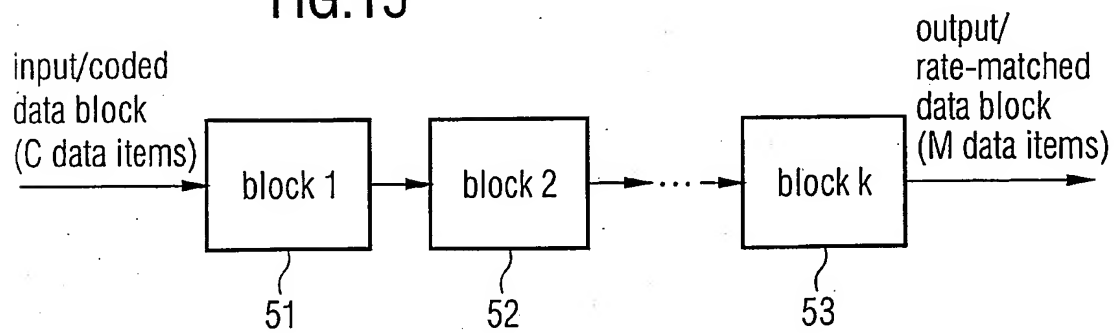
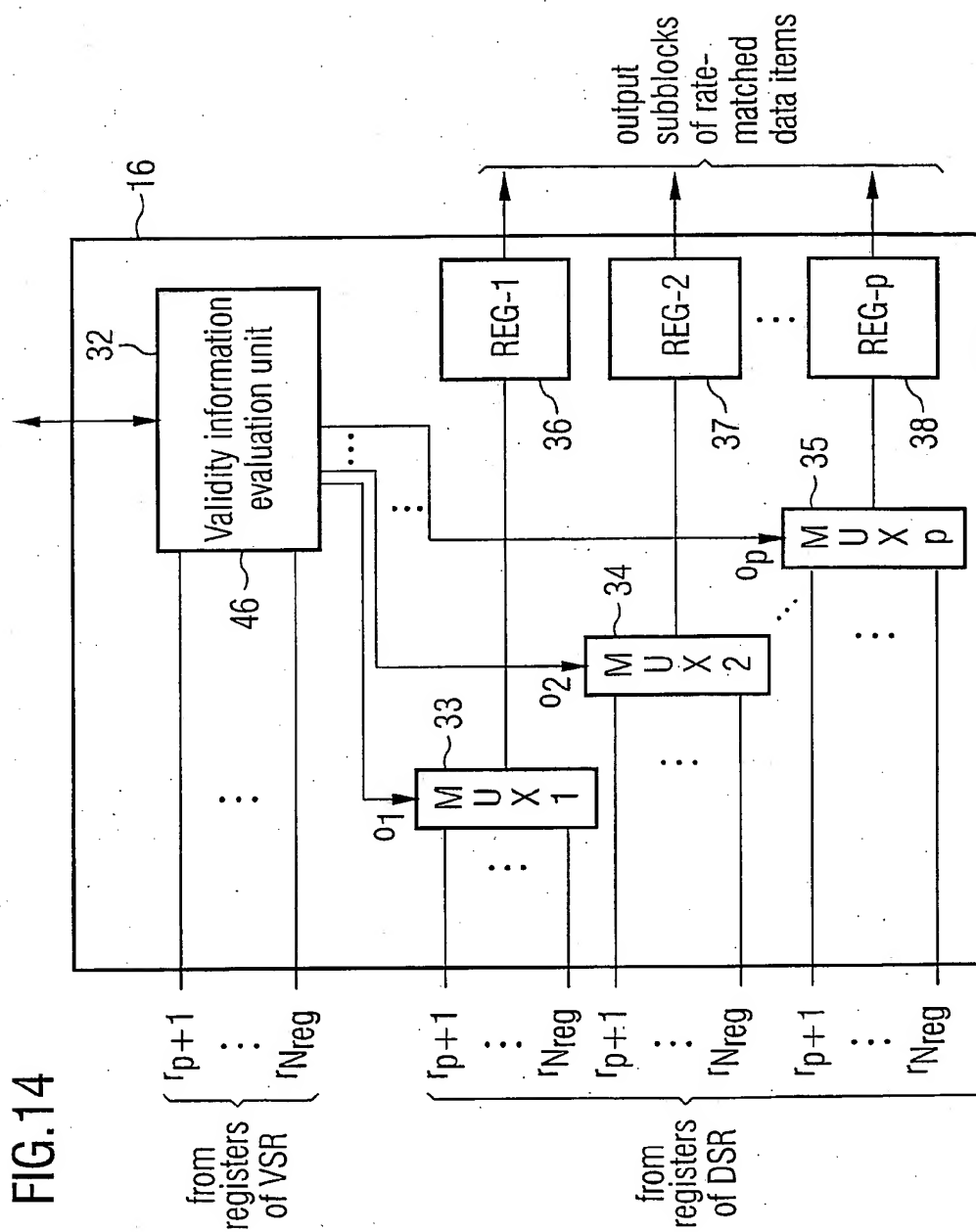


FIG. 14



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FIG.16a

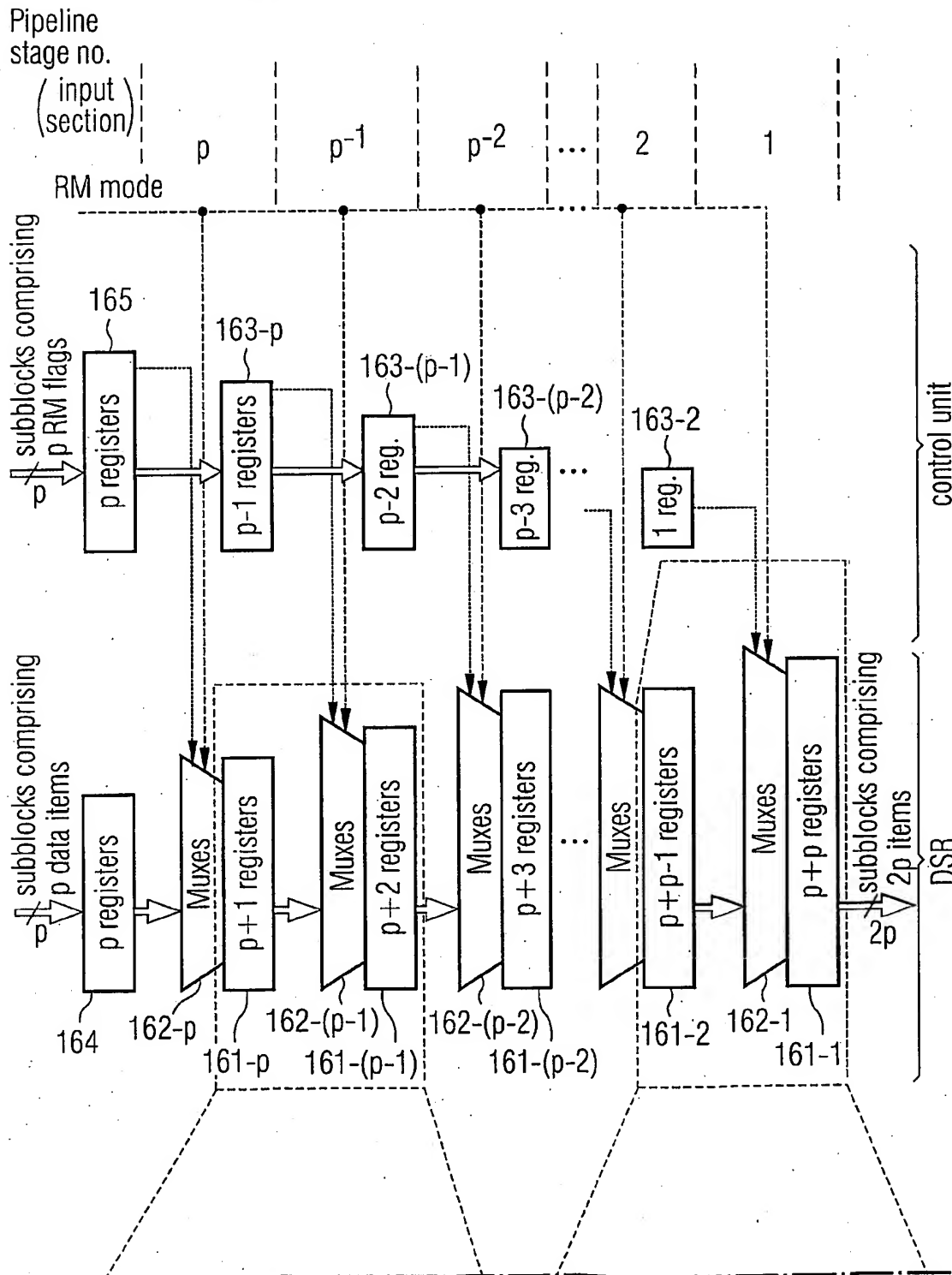


FIG.16b

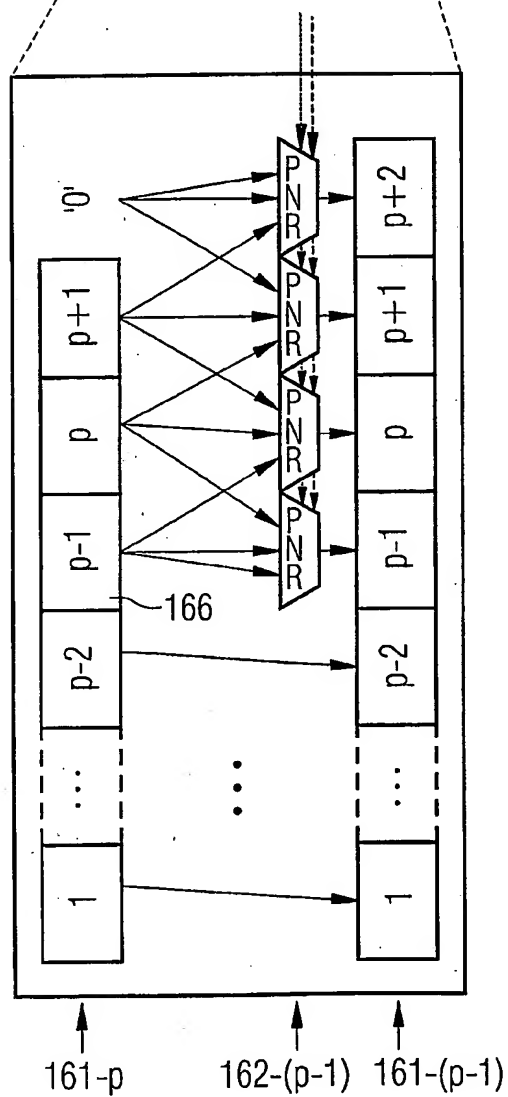
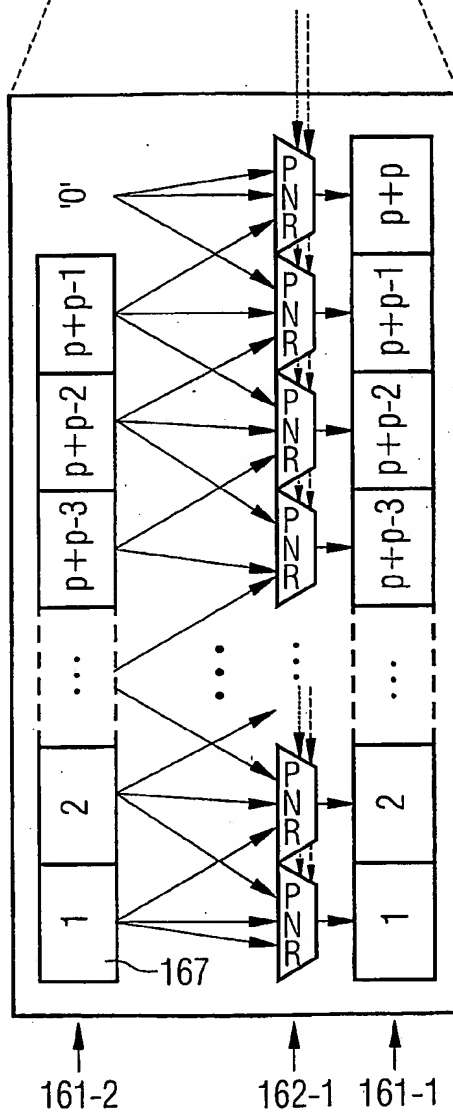


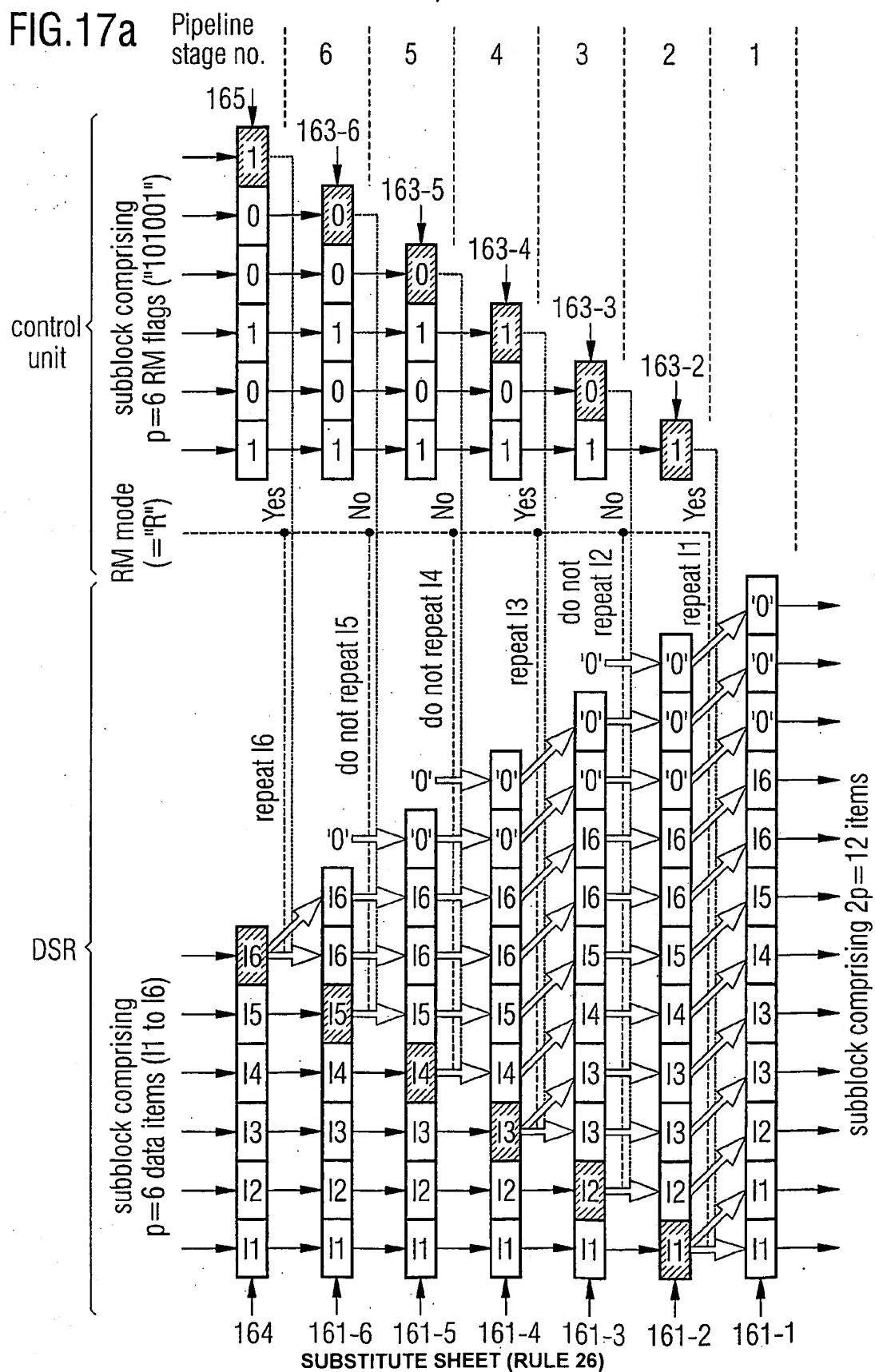
FIG.16c

Legend:

- \boxed{j} : j-th register of DSR
- ∇ : multiplexer

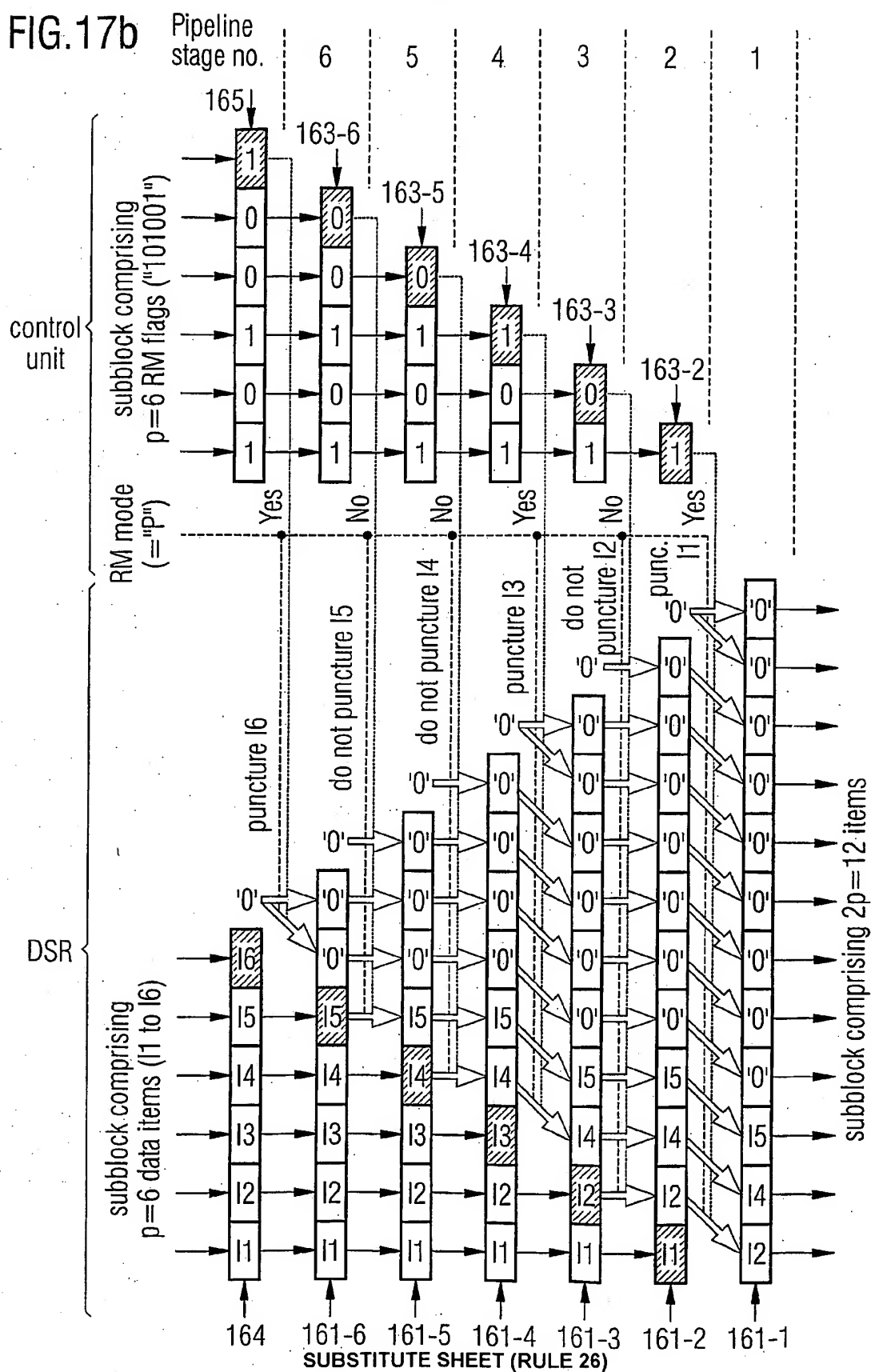
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FIG.17a



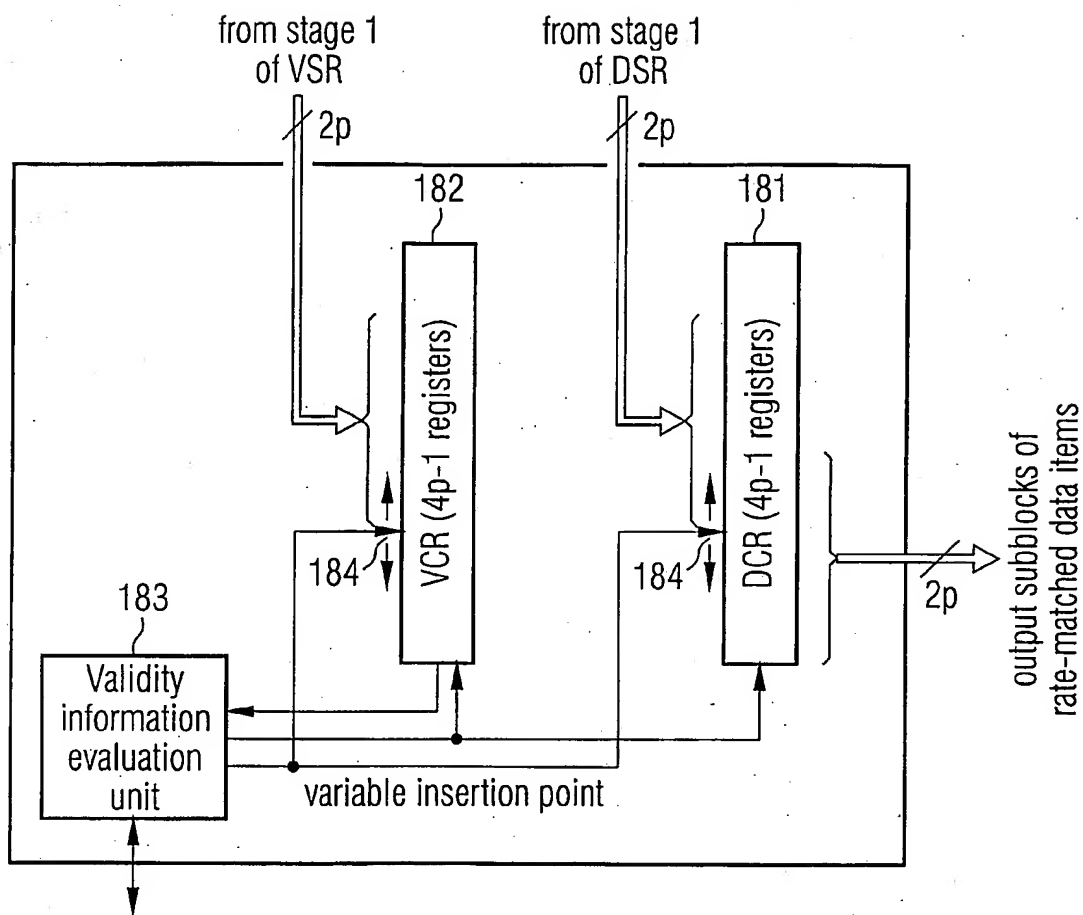
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FIG. 17b



SUBSTITUTE SHEET (RULE 26)

FIG.18a



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FIG.18d

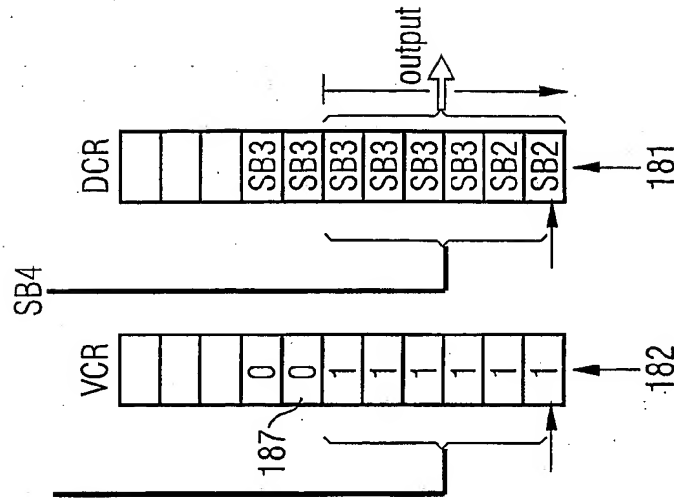


FIG.18c

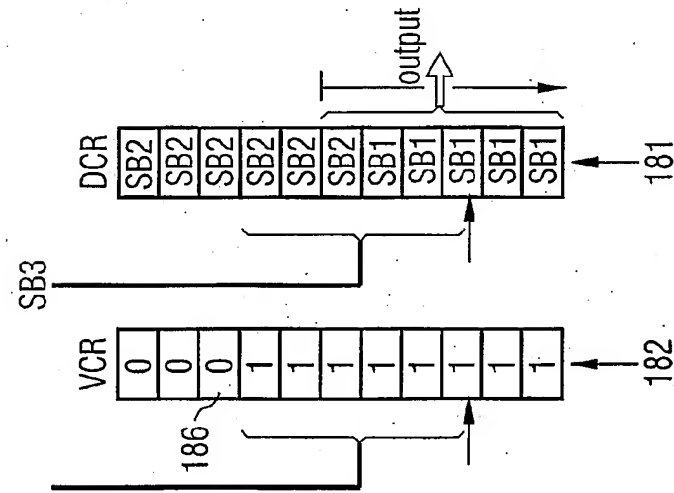


FIG.18b

